REMARKS

Applicant respectfully requests allowance of the subject application.

Claims 1-10, 12, 20, 24-41, 47, 51-55 and 68 are cancelled.

Claims 11, 13-19, 21-23, 42-46 and 48-50 and 56-67 are pending.

In view of the following remarks, Applicant respectfully requests that the rejections be withdrawn and the application be forwarded along to issuance

§§ 102(b) Rejection

Claims 11, 13-17, 19, 42-46 and 48-50 and 56-67 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,560,676 to Nishimoto et al. (hereinafter "Nishimoto"). The Applicant respectfully disagrees.

Claim 11 recites a method comprising:

- querying whether a set of data resides in a cache memory that is communicatively coupled to a processor unit;
- receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory; and
- communicating the indication to an operating system being executed on the processor unit.

Nishimoto does not disclose these features.

The Examiner, in rejecting claim 11, asserts ""communicating the indication to an operating system being executed on the processor is equivalently taught as the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the operating system within the processor (e.g., see

column 5, lines 62-65)." *See Office Action Dated January 17, 2006, Page 7.* The asserted portion is excerpted as follows for the sake of convenience:

> Using the select signal 118, the selector 108 selects a piece of data and a tag from 4 pieces of data and 4 tags read at the same time, and outputs read data 114 and a read tag 115 as a result of the load instruction. *See Nishimoto, Col. 5, Lines 65-65.*

In neither the above referenced portion, nor elsewhere in Nishimoto, is "communicating the indication to an operating system being executed on the processor unit" as recited in Claim 11 disclosed. Indeed, the words "operating system" are not even included within the text of Nishimoto.

As the Examiner is well aware, anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). In the present case, the Examiner seems to be applying an "equivalence" standard, the support for which is unclear to the Applicant and is respectfully submitted to be in error.

The Applicant respectfully requests that the Examiner state with specificity as to which element of Nishimoto is being asserted as the "operating system" of Claim 11. As the Examiner is also aware, "[w]here a major technical rejection is proper, it should be stated with a full development of reasons rather than by a mere conclusion coupled with some stereotyped expression." *M.P.E.P. §707.07(g)* Regardless, because each element of Claim 11 (e.g., an operating system) is not included in Nishimoto, it is respectfully submitted that a *prima facie* case of

anticipation has not been established and withdrawal of the rejection is respectfully requested.

Claims 42 and **63** are also independent claims and are allowable based on the reasons recited above. As previously described, Nishimoto does not even include the words "operating system". Therefore, Nishimoto cannot disclose "communicating the indication to ***an operating system*** being executed on the processor unit" as recited in Claim nor "communicate a result of the determination to ***an operating system*** being executed on the processor chip" as recited in claim 63. Accordingly, withdrawal of the rejection with respect to Claims 42 and 63 is also respectfully requested.

Claims 13-18 depend either directly or indirectly from Claim 11 and are allowable as depending from an allowable base claim. **Claims 43-44** depend either directly or indirectly from Claim 42 and are allowable as depending from an allowable base claim. **Claims 64-67** depend either directly or indirectly from Claim 42 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in their respective independent claims, are neither shown nor suggested in the references of record, either singly or in combination with one another. Withdrawal of the rejection is respectfully requested.

Claim 19 recites a method comprising:

- comparing an address of a set data with at least one other address in a cache memory, wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;

- providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included;
- establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included; and
- communicating the indication, by the processor unit, to software being executed on the processor unit.

Nishimoto does not disclose these features.

Beginning at page 10 of the subject Application, exemplary execution of a residency instruction is described. An execution of the residency instruction is used to improve the interaction of the processor chip with the cache memory, and more particularly, to improve performance of software being executed on the processor chip. The residency instruction, when executed on the processor chip, is used to determine if a set of data resides in the cache memory. Through execution of the residency instruction, the processor chip may recognize characteristics likely to be encountered when accessing the set of data. For example, characteristics of data access may include whether the set of data resides in the cache memory, and therefore may be accessed with minimal delay, or whether the set of data resides in other portions of the memory, such as RAM, peripheral memory, and the like. Therefore, the processor chip may establish a relative amount of time it will take to access the set of data, without actually accessing the set of data, e.g., reading or writing the set of data. The processor chip may communicate a result of the determination to software being executed on the

processor chip such that the software may use the result to plan the next actions to be performed when executing the software. For instance, the software may determine which operation to perform first based on whether a set of data that will be the subject of the operation is available from the cache memory.

In some instances, a cache memory may include a plurality of levels. For instance, beginning at page 12 of the subject Application, each of the levels of the cache memory may be configured to provide different functionality when used in conjunction with the processor unit. For example, the level one cache memory may provide access to data stored in the level one cache memory at a rate which is equal to or close to the processor unit's speed, e.g. an amount of time taken to execute an instruction by the processor unit. The level two cache memory may be configured to store a greater amount of data than the amount of data stored in the level one cache memory. The level two cache memory, however, may provide access to data at a slower rate than the level one cache memory. *See subject Application, Page 12 and FIG. 2.*

The Examiner, in the rejection of Claim 19, asserts FIGS. 3 and 4 of Nishimoto and column 4, lines 31 et seq. as disclosing a cache memory having a plurality of levels, the portions of which are excerpted as follows for the sake of convenience:

> FIG. 3 is a schematic block diagram of cache memory system 100. According to this embodiment, the cache memory system has a cache size of 128K bytes and a block size of 128 bytes, and employs a 4-way set associative system. The cache memory system uses LRU as a block replacement

> algorithm, and is controlled by a store through method. TI should be noted that in the figure, portions of the load/store unit 18 not related to the present invention are not shown. *See Nishimoto, Col. 4, lines 40-48.*

However, neither the above excerpted portion, the asserted figures nor elsewhere in Nishimoto is a cache memory having different levels disclosed. Rather, the above referenced portion clearly describes a single-level cache memory. Accordingly, since each claimed element (e.g., cache memory having a plurality of levels) is not disclosed in Nishimoto, it is respectfully submitted that a *prima facie* case of anticipation has not been established and withdrawal of the rejection is respectfully requested.

Claims 21-23 depend either directly or indirectly from Claim 19 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in their respective independent claim, are neither shown nor suggested in the references of record, either singly or in combination with one another. Withdrawal of the rejection is respectfully requested.

Claim 45 recites a system comprising:

- a cache memory; and
- a processor unit communicatively coupled to the cache memory, wherein the processor unit includes a cache residency test instruction that, when executed, configures the processor unit:
  - to query whether a set of data resides in the cache memory;
  - to receive an indication from the query of whether the set of data resides in the cache memory;
  - to establish a relative amount of time to access the set of data; and
  - to communicate the indication and the relative amount of time to software being executed on the processor unit.

Nishimoto does not disclose these features.

The Examiner first asserts that "the indication to software being executed on the processor unit is taught as when the data resides the cache (cache hit), a '1' is outputted as a hit signal 116". *See Office Action Dated January 17, 2006, Page 15.* The Examiner then asserts that "when a central processing unit is referring to data and instructions from a particular space within physical memory, it will most probably, once again, refer to the data and instructions from that space (temporal locality; e.g. see column 2, lines 20 et seq.) wherein the process have to establish amount of time to access said set of data; and the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65)". *See Office Action Dated January 17, 2006, Page 16.* First of all, it is respectfully submitted that a standard of "it will most probably" asserted by the Examiner is clearly not within the standard of anticipation nor even obviousness. As previously described, anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration, not that the reference "will most probably" include the element. The Applicant respectfully requests that the Examiner further explain with specificity as to how the asserted portions disclose the claimed features.

Regardless, the Applicant respectfully submits that the above recited features are not disclosed by Nishimoto. The only mention of read data and read tag in Nishimoto is described as follows:

> The select way control circuit 113 determines the way to be read according to a determination result by the hit/miss determination circuit 122. When the determination result is a

> cache hit (the hit signal 116 is "1"), the select way control circuit 113 outputs the way number indicated by the hit way signal 119, as a select way signal 117. This select way signal 117 is also used as a select signal 118 to the selector 108. Using the select signal 118, the selector 108 selects a piece of data and a tag from 4 pieces of data and 4 tags read at the same time, and outputs read data 114 and a read tag 115 as a result of execution of the load instruction. *See Nishimoto, Col. 5, Lines 55-65.*

As shown in the above excerpted portion, however, neither the read data nor the read tag "communicate **the indication and the relative amount of time** to software being executed on the processor unit" as recited in Claim 45.

Accordingly, since each claimed element is not disclosed in Nishimoto, it is respectfully submitted that a *prima facie* case of anticipation has not been established and withdrawal of the rejection is respectfully requested.

Claim 56 is also an independent claim and is allowable based on the reasons recited above. As previously described, Nishimoto does not communicate the indication and the relative amount of time. Accordingly, withdrawal of the rejection with respect to Claim 56 is also respectfully requested.

Claims 46, 48-50 depend either directly or indirectly from Claim 45 and are allowable as depending from an allowable base claim. **Claims 57-62** depend either directly or indirectly from Claim 56 and is allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in their respective independent claim, are neither shown nor suggested in the references of record, either singly or in combination with one another. Withdrawal of the rejection is respectfully requested.

Conclusion

All of the claims are in condition for allowance. Accordingly, Applicant requests a Notice of Allowability be issued forthwith. If the Office's next anticipated action is to be anything other than issuance of a Notice of Allowability, Applicant respectfully requests a telephone call for the purpose of scheduling an interview.

Respectfully Submitted,

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